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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,019	10/28/2003	Kenichi Takahara	117268	3712

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EXAMINER	
VU, PHU	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,019	TAKAHARA ET AL.	
	Examiner	Art Unit	
	Phu Vu	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,3-9,11-19,21 and 22 is/are pending in the application.

4a) Of the above claim(s) 9,11,13-17 and 22 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3-8,11,12,18,19 and 21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/25/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: Foreign Patent Document.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of species IA and IIA is acknowledged. The traversal is on the ground(s) that the search is not burdensome. This is not found persuasive because differences between the species are significant enough that requires additional search that proves to be a burden when searching.

The requirement is still deemed proper and is therefore made FINAL.

Allowable Subject Matter

The indicated allowability of claims 9-11 and 13-19 are withdrawn in view of the newly discovered reference(s) to Takashi (see below). Rejections based on the newly cited reference(s) follow.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, 14, 15, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Takashi JP2002-215064.

Regarding claims 11, Takashi teaches an electro-optical device comprising, above a substrate: data lines (fig. 2 element 6a) extending in a first direction; scanning lines (3a) extending in a second direction and intersecting the data lines; pixel electrodes (9a) and thin film transistors (fig. 1 3a is the gate of the TFT) disposed so as to correspond to intersection regions of the data lines and the scanning lines; and storage capacitors (fig. 7 element 70) electrically connected to the thin film transistors and the pixel electrodes. Takashi also teaches the storage capacitor having a dielectric multilayer film comprising a high temperature oxide of 5-200 nm thickness and a Low temperature oxide film or a silicon nitride film. Therefore since the materials are different one must exhibit a higher dielectric constant than the others. The reference also teaches TFTs including semiconductor layers having channel regions (fig. 8 1a') which extend in a longitudinal direction and channel adjacent regions (near 83 and 81) which extend in the longitudinal direction further from the channel region. The reference also shows scanning lines including main body parts extending in a direction intersecting the longitudinal direction (3a) and having gate electrodes overlapping the channel regions in plan view (see figs 7 and 8 element 3a and 1a') and horizontal (3b') protrusions protruding from the main body parts in the longitudinal direction at sides of the channel adjacent regions in plan view.

Regarding claims 14, Takashi teaches an electro-optical device comprising, above a substrate: data lines (fig. 2 element 6a) extending in a first direction; scanning lines (3a) extending in a second direction and intersecting the data lines; pixel electrodes (9a) and thin film transistors (fig. 1 3a is the gate of the TFT) disposed so as

to correspond to intersection regions of the data lines and the scanning lines; and storage capacitors (fig. 7 element 70) electrically connected to the thin film transistors and the pixel electrodes. Takashi also teaches the storage capacitor having a dielectric multilayer film comprising a high temperature oxide of 5-200 nm thickness and a Low temperature oxide film or a silicon nitride film. Therefore since the materials are different one must exhibit a higher dielectric constant than the others. The reference also teaches TFTs including semiconductor layers having channel regions (fig. 8 1a') which extend in a direction. The reference also shows scanning lines including main body parts (3a) and having gate electrodes facing the channel regions(see figs 7 and 8 element 3a and 1a') with gate insulating films (fig. 7 element 2) interposed therebetween and extending in the second direction which intersects the first direction in plan view and vertical protrusions (fig. 11 3c') protruding downwardly from the main line portions at positions which are separated from the channel region by a predetermined distance in the second direction in plan view.

Regarding claim 15, Takashi teaches lower light-shielding film (11a')s which cover at least the channel regions from the lower side; and the vertical protrusions contacting the channel regions at a lower side (see fig. 11)

Regarding claim 18, Takashi teaches an electro-optical device comprising, above a substrate: data lines (fig. 2 element 6a) extending in a first direction; scanning lines (3a) extending in a second direction and intersecting the data lines; pixel electrodes (9a) and thin film transistors (fig. 1 3a is the gate of the TFT) disposed so as to correspond to intersection regions of the data lines and the scanning lines; and

storage capacitors (fig. 7 element 70) electrically connected to the thin film transistors and the pixel electrodes. Takashi also teaches the storage capacitor having a dielectric multilayer film comprising a high temperature oxide of 5-200 nm thickness and a Low temperature oxide film or a silicon nitride film. Therefore since the materials are different one must exhibit a higher dielectric constant than the others. The limitation of a pixels of a electrode groups driven inversely at a first period and a second group driven inversely at a second period complementary to the first period is a product-by-process limitation. Product-by-process limitations are limited only to the structure that the process implies. The driving method does not appear to structurally limit the claim to any structure other than having pixels arranged in a plane, which the reference teaches (see fig. 2). The reference also teaches data lines (fig. 2 6a) including main line portions which are extended to upper sides of the scanning lines so as to intersect the scanning lines and overhanging portions (fig. 5 element 71) which overhang along the scanning lines, a counter electrode (fig. 3 element 22) which faces the plurality of pixel electrodes on a counter substrate which is provided opposite to the substrate; and convex portions (see fig. 5) formed on base surfaces of the pixel electrodes on the substrate corresponding to the overhanging portions, the convex portions being regions of gaps between the pixel electrodes, which are adjacent to each other with the scan lines interposed between them.

Regarding claim 19, Takashi teaches an electro-optical device comprising, above a substrate: data lines (fig. 2 element 6a) extending in a first direction; scanning lines (3a) extending in a second direction and intersecting the data lines; pixel

electrodes (9a) and thin film transistors (fig. 1 3a is the gate of the TFT) disposed so as to correspond to intersection regions of the data lines and the scanning lines; and storage capacitors (fig. 7 element 70) electrically connected to the thin film transistors and the pixel electrodes. Takashi also teaches the storage capacitor having a dielectric multilayer film comprising a high temperature oxide of 5-200 nm thickness and a Low temperature oxide film or a silicon nitride film. Therefore since the materials are different one must exhibit a higher dielectric constant than the others. The limitation of a pixels of a electrode groups driven inversely at a first period and a second group driven inversely at a second period complementary to the first period is a product-by-process limitation. Product-by-process limitations are limited only to the structure that the process implies. The driving method does not appear to structurally limit the claim to any structure other than having pixels arranged in a plane, which the reference teaches (see fig. 2). Takashi teaches a counter electrode (fig. 3 element 22) which faces the plurality of pixel electrodes on a counter substrate which is provided opposite to the substrate; the convex portions having gentle step differences (see figure 5). The limitation of convex portions "formed by removing planarization films which are formed in advance on the convex portions by an etching process and causing the surfaces of the convex portions which are exposed after removing to be receded" is also a product by process limitation that appears to only limit the convex portions being receded which the reference teaches (see fig 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 8, 12 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et. al US Publication No. 2002/0018278 in view of Sato (Sato B) 20030016311 in view of Ohtani 6088070.

Regarding claims 1 and 21, Sato teaches an electro-optical device comprising, above a substrate (figure 17 element 10), data lines (figure 2 element 6a) extending in first direction, scanning lines extending (fig. 2 element 3a) in a second direction which intersect the data lines pixel electrodes (fig. 2 element 9a), storage capacitors electrically connected to the TFT (figure 17 element 70) The reference fails to teach the light shielding layer covering the entire data lines in plan view however, the reference does teach a light shielding layer between the pixel electrode and the data lines covering the data lines and wider than the data lines. Sato teaches forming a light shield (see fig. 4 and 5O element 10) covering the entire data lines and between the pixel electrode (see fig. 5O element 12) and the data line as prevent light from irradiating in the LDD regions inducing a leakage current. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to extend Sato's light shield in order to cover the entire data line to further reduce leakage current. The references also fail to teach the dielectric films which constitute the storage capacitors being made

of a plurality of layers including different materials and also of one of the plurality of layers being made of a material having a higher dielectric constant however they do teach mulilayer dielectric layers and a plurality of material choices for he layers (figure 17 element 75') and (see [0098]). Ohtani teaches a multi-layer dielectric used in a capacitor comprising of a silicon oxide and nitride film, the oxide serving as a coating layer (column 3 lines 1-10). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to apply a silicon oxide layer to a nitride dielectric layer to serve as a coating (protection) for the nitride layer.

Regarding claim 3, the reference teaches a dielectric layer being formed of silicon nitride (see column 13 lines 45-50).

Regarding claim 4, the reference teaches the storage capacitor (fig. 17 element 70) being formed above semiconductor layers (fig. 17 element 1a) and below pixel electrodes (fig. 17 element 9a).

Regarding claim 5, the limitation of a planarization process performed on the interlayer insulating film positioned beneath the pixel electrodes is a product-by-process limitation. Product-by-process limitations are limited only to the structure that the process implies. Since the insulator film is substantially flat (43 see fig. 7) than this meets the limitation of the claim.

Regarding claim 8, the shielding layer is also formed of the same film as the relay layer (see figure 17 element 71a').

Regarding claim 12, the reference teaches the TFT semiconductor layers having channel regions which extend in a longitudinal direction (see fig 17 element 3a),

an upper light-shielding film covering at least the channel regions of the TFT from the upper side (see fig. 17 element 300') and at least part of the upper-light shielding films formed in a concave shape in the cross section which is perpendicular to the longitudinal direction of the channel regions as viewed from the channel regions (fig 17 element 300' – region directly above 3a).

Claims 6-7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato in view of Sato B in view of Ohtani and further in view of Yoshida 5734455.

Regarding claim 6, teach all the limitations of claim 6 except one of the electrodes of the storage capacitors made of the same material as the data lines. Takashi teaches the data lines made of aluminum (see [0002]), however does not specify a material for the storage capacitor electrode. Yoshida teaches that it is conventional to form storage electrodes of aluminum (see column 2 lines 60-65). Conventionality has associative benefits such as well developed implementations and lower costs. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use aluminum as the material for the storage capacitor electrode to gain benefits of conventionality.

Regarding claim 7, the reference teaches relay layers (71 fig. 17) connecting the pixel electrodes to one pair of the storage capacitor electrodes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562. The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571)-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Vu
Examiner
AU 2871

ANDREW SCHECHTER
PRIMARY EXAMINER